



## ST16N10



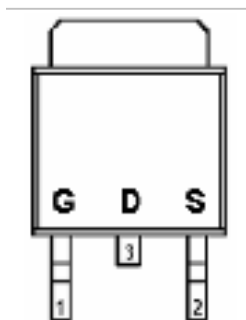
N Channel Enhancement Mode MOSFET

16.0A

### DESCRIPTION

ST16N10 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The ST16N10 has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### PIN CONFIGURATION TO-252



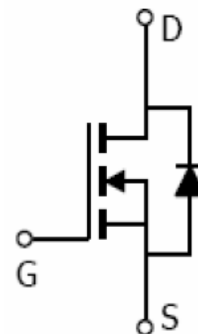
### FEATURE

- 100V/16.0A,  $R_{DS(ON)} = 140m\Omega$  (Typ) @ $V_{GS} = 10V$
- 100V/6.0A,  $R_{DS(ON)} = 160m\Omega$  (Typ) @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 Package design

### PART MARKING



**Y: Year Code**  
**A: Date Code**  
**B: Wafer Code**



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**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	100	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	16.0 8.0	A
Pulsed Drain Current	IDM	50	A
Continuous Source Current (Diode Conduction)	IS	15	A
Power Dissipation	PD	79	W
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	110	°C/W



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**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250mA$	100			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$			25	uA	
		$V_{DS}=80V, V_{GS}=0V$ $T_J=150^\circ C$			250		
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	50			A	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=16A$		140	150	mΩ	
		$V_{GS}=4.5V, I_D=6A$		160	170		
Forward Transconductance	$g_{fs}$	$V_{DS}=50V, I_D=9.0A$	6.4			S	
Diode Forward Voltage	$V_{SD}$	$I_S=9.0A, V_{GS}=0V$			1.2	V	
<b>Dynamic</b>							
Total Gate Charge	$Q_g$	$V_{DS}=80V, V_{GS}=10V$ $I_D=9.0A$			45	nC	
Gate-Source Charge	$Q_{gs}$				7.2		
Gate-Drain Charge	$Q_{gd}$				22		
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS}=0V$ $F=1MHz$		640		pF	
Output Capacitance	$C_{oss}$			160			
Reverse Transfer Capacitance	$C_{rss}$			88			
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_D= 5.5\Omega$ $I_D=9.0A, V_{GEN}=10V$ $R_G=12\Omega$		7.4		nS	
	$t_r$			29			
Turn-Off Time	$t_{d(off)}$				40		
	$t_f$				25		

**TYPICAL CHARACTERISTICS**

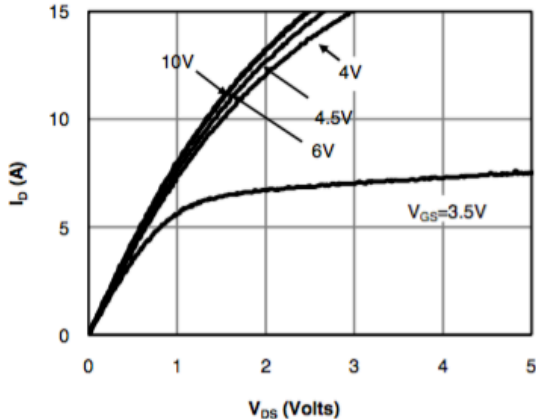


Fig 1: On-Region Characteristics (Note E)

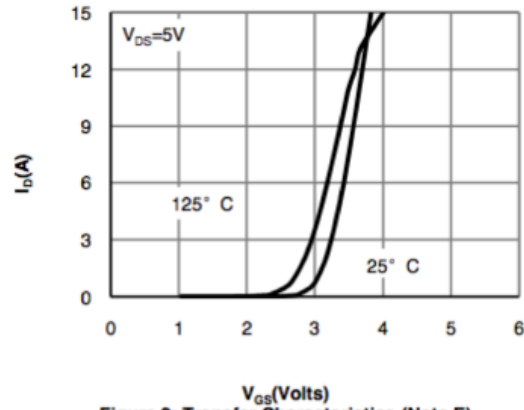


Figure 2: Transfer Characteristics (Note E)

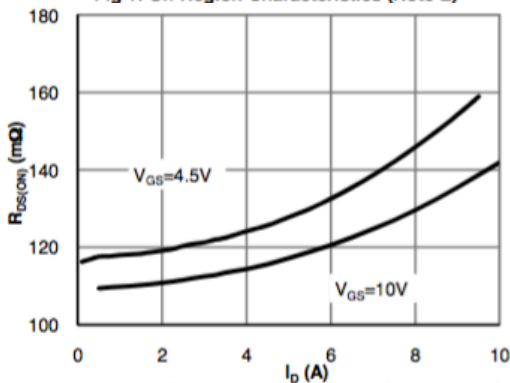


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

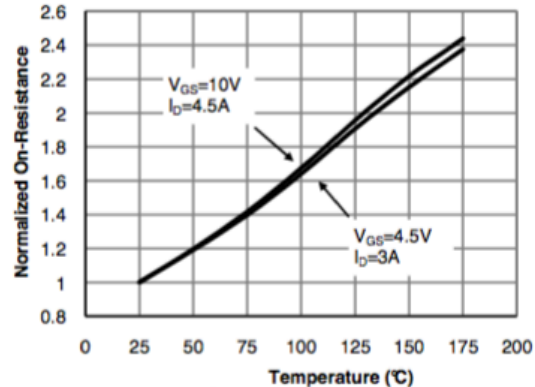


Figure 4: On-Resistance vs. Junction Temperature (Note E)

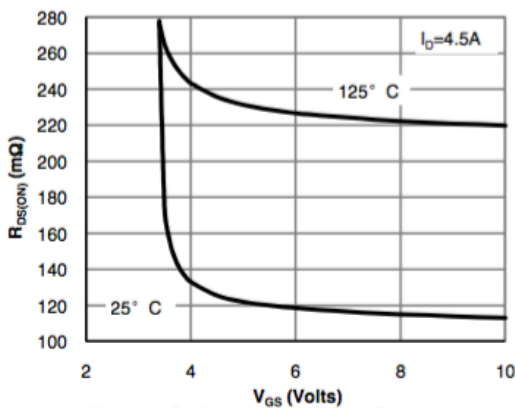


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

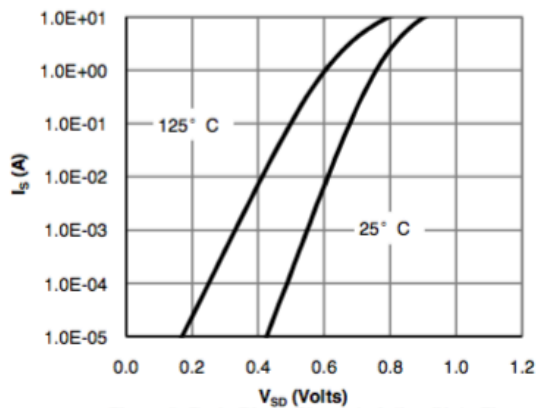


Figure 6: Body-Diode Characteristics (Note E)

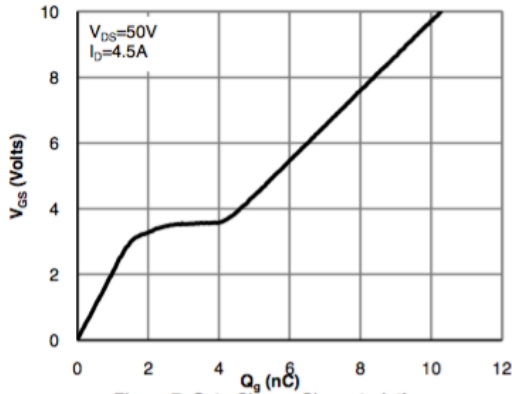
**TYPICAL CHARACTERISTICS**


Figure 7: Gate-Charge Characteristics

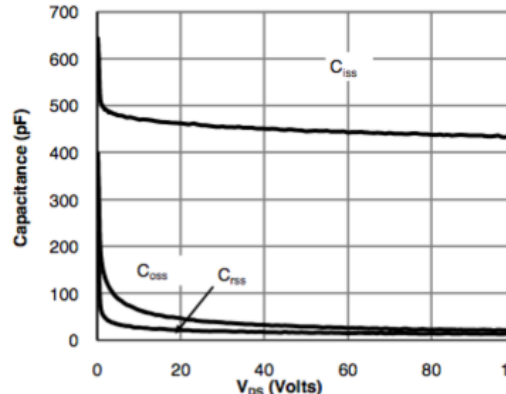


Figure 8: Capacitance Characteristics

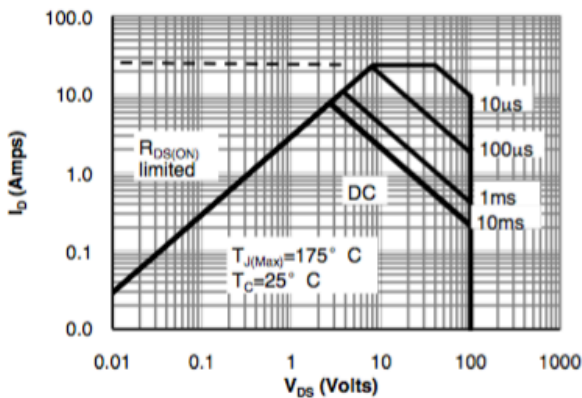


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

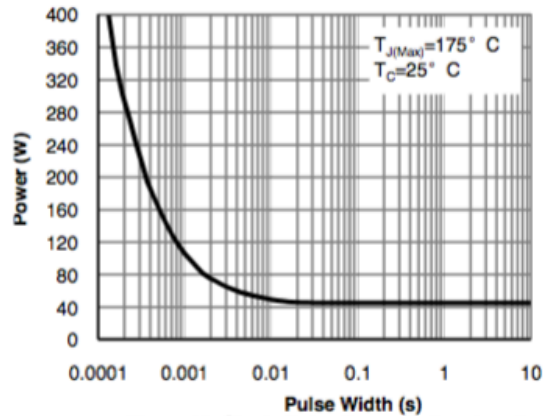


Figure 10: Single Pulse Power Rating Junction-Case (Note F)

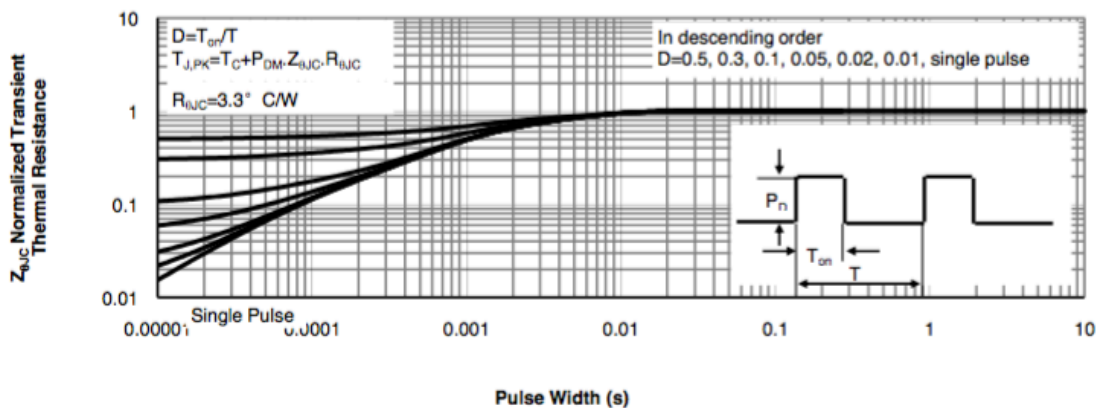


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL CHARACTERISTICS**

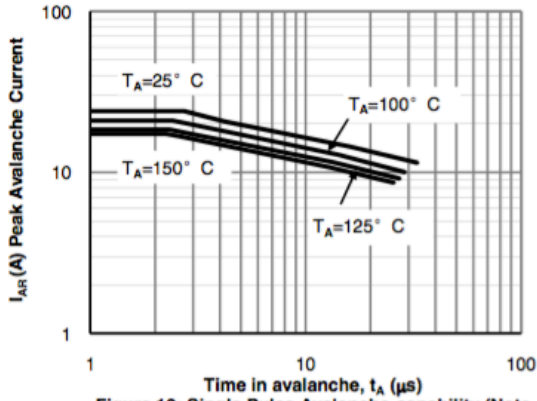


Figure 12: Single Pulse Avalanche capability (Note C)

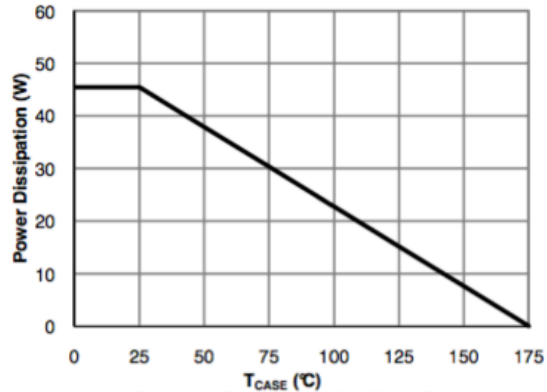


Figure 13: Power De-rating (Note F)

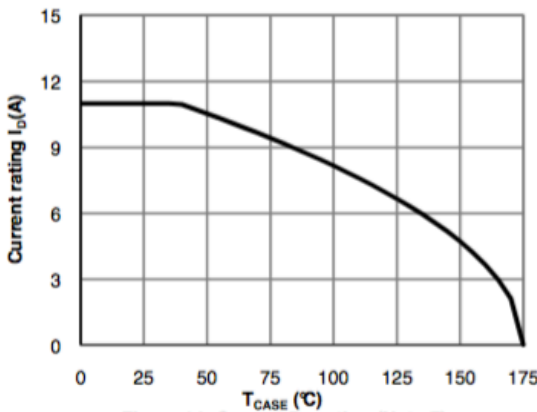


Figure 14: Current De-rating (Note F)

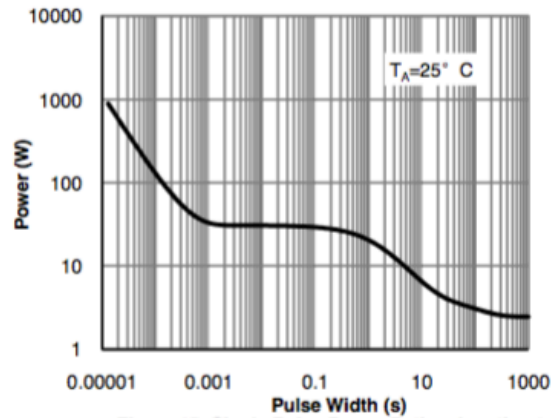


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

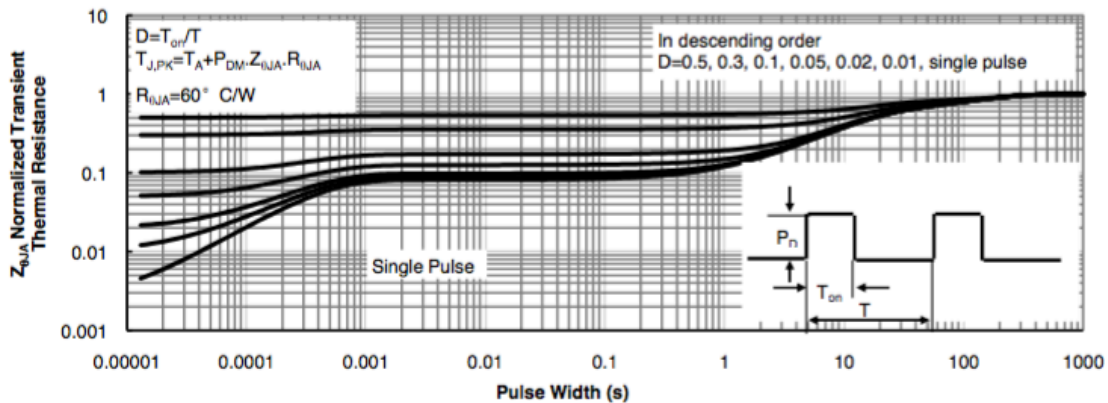


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

**TO-252-2L PACKAGE OUTLINE**

